## Neuromorphic Hardware in Practice and Use

**Organizers**

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**Description of the workshop**

*Abstract*

This workshop is designed to explore the current advances, challenges and best practices for working with and implementing algorithms on neuromorphic hardware. Despite growing availability of prominent biologically inspired architectures and corresponding interest, practical guidelines and results are scattered and disparate. This leads to wasted repeated effort and poor exposure of state-of-the-art results. We collect cutting edge results from a variety of application spaces providing both an up-to-date, in-depth discussion for domain experts as well as an accessible starting point for newcomers.

*Goals & Objectives*

This workshop strives to bring together algorithm and architecture researchers and help facilitate how challenges each face can be overcome for mutual benefit. In particular, by focusing on neuromorphic hardware practice and use, an emphasis on understanding the strengths and weaknesses of these emerging approaches can help to identify and convey the significance of research developments. This overarching goal is intended to be addressed by the following workshop objectives:

1) Explore implemented or otherwise real-world usage of neuromorphic hardware platforms

2) Help develop 'best practices' for developing neuromorphic-ready algorithms and software

3) Bridge the gap between hardware design and theoretical algorithms

4) Begin to establish formal benchmarks to understand the significance and impact of neuromorphic architectures

*Relevance to IEEE WCCI*

IJCNN covers a wide range of topics in the field of neural networks and neural computation. In recent years, these topics have expanded to include biologically inspired hardware implementation research as well. The rapidly evolving need for hardware accelerators to enable the algorithmic and theoretical advances being made by WCCI attendees and participants also necessitates an understanding of how the interplay of algorithms and architectures in the form of neuromorphic computation is advantageous. A better understanding of the algorithm and architecture interplay also allows for the development of meaningful benchmarking which can further highlight the significance of research advances.

We expect three primary groups to comprise the audience.

1. **Neuromorphic Hardware Experts:** Recently a new field of neuromorphic platforms has become available, either at prototype or release stages. These platforms originate from a variety of groups within industry, academia and government. Hardware designers and platform stakeholders have a keen interest in early adoption, algorithms and applications as well as comparative and case studies.
2. **Spiking Neural Network Algorithm Designers:** As is evidenced by the growing presence of spiking neural networks at conferences such as IJCNN, biologically inspired spiking neural networks offer new and expanding capabilities. However, these algorithms are rarely designed following particular hardware constraints, and this creates a challenge when implementing the algorithms in practice. By expounding on neuromorphic implementations of spiking networks, algorithm designers stand to expand both utility and practicality.
3. **Low-Power and Embedded Application Spaces:** Neuromorphic platforms offer compelling improvements in performance-per-Watt. However, these numbers are often vendor-supplied and rarely include difficulties involved with algorithm porting. This workshop will offer a true-to-life story of the process, benefits and pitfalls of using neural networks on these up-and-coming platforms.

**Scope and Topics:**

Neuromorphic hardware; benchmarks and comparisons; applications, software, and toolkits; algorithms; workflows and integration

**Workshop duration, format, activities, and schedule**

This half day workshop will consist of a brief overview of the various approaches to neuromorphic computation and motivate the need for applied results and benchmarks to properly characterize the significance of such approaches. Following the introduction will be a series of talks interleaving invited keynote speakers and contributed talks. A poster and demonstration session will conclude the session while encouraging discussion amongst the participants.

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| 13:00 - 13:20 | Welcome and Opening Overview Talk |
| 13:20 – 13:50 | Invited Talk |
| 14:00 – 14:20 | Contributed talk |
| 14:20 – 14:40 | Contributed talk |
| 14:40 – 15:00 | Contributed talk |
| 15:00 - 15:15 | Break |
| 15:15 – 15:45 | Invited Talk |
| 15:45 – 16:00 | Contributed talk |
| 16:00 – 16:15 | Contributed talk |
| 16:15 – 16:30 | Contributed talk |
| 16:30 – 17:00 | Invited Talk |
| 17:00 – 17:30 | Posters & Demonstrations |

*Submission Guidelines and Timeline*

The workshop requests submissions to follow IEEE conference style similar to the main conference. Papers should be submitted in pdf format with a maximum length of 2 pages (excluding references and acknowledgements). Appendices are not permitted beyond the 2 page limit. Submissions will be selected according to reviewer's comments and scoring with emphasis on quality, novelty, appropriateness for the workshop and potential impact on the field.

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| 30 April 2018 | Workshop submission deadline |
| 1 May 2018 | Submissions sent to reviewers |
| 10 May 2018 | Decisions sent to submission authors |